OIPE JC123
JAN 29 2003
PATENT & TRADEMARK OFFICE

APPENDIX A - AMENDMENTS TO THE CLAIMS

The following claims have been amended by deleting the bracketed ("[ ]") portions and adding the underlined ("__") portions.

1. (Amended) A method for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in an instruction reordering mechanism of a processor that can launch execution of instructions out of order via a predefined number of ports, comprising the steps of:

(a) providing said instruction reordering mechanism having a plurality of said instructions, each said instruction having a respective logic element for causing and preventing launching, when appropriate, of said instruction; and

(b) propagating a set of signals successively during a launch cycle through said logic elements of said instruction reordering mechanism that causes said logic elements to track which of the predefined plurality of said instructions are launched and causes the selection of no more than said predefined number of ports during said launch cycle [launch said predefined plurality of said instructions].

13. (Amended) A system for finding a predefined plurality of instructions, if available, that are ready to be executed in a processor that can launch execution of instructions out of order, comprising:

(a) an instruction reordering mechanism for temporarily storing a plurality of said instructions; and

(b) a plurality of logic elements associated with said instruction reordering mechanism and associated respectively with each of said instructions in said instruction reordering mechanism for causing and preventing launching, when appropriate, of respective instructions, said logic elements configured to propagate a plurality of signals monotonically [for propagating successively] through said logic elements [a plurality of signals] that causes said logic elements to select said predefined plurality of said instructions for launching and to de-select any remaining instructions during a launch cycle.

23. (Amended) A system for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in a queue of a processor that can launch execution of instructions out of order, comprising:

(a) queue means for storing a plurality of said instructions, said queue means having a plurality of launch logic means for causing and preventing launching, when appropriate, of a respective instruction; and

(b) logic means associated with said queue, said logic means for propagating during a launch cycle a set of signals [successively] monotonically to successive launch logic means to indicate both when and which of one or more ports of one or more execution resources are available for each said instruction and when none of said ports are available.